REMARKS

In view of the above amendments and the following remarks, reconsideration of the rejections contained in the Office Action of December 12, 2006 is respectfully requested.

By this Amendment, claims 1, 9, 14 and 15 have been amended, and claims 11-13, 16 and 19-20 have been cancelled. Thus, claims 1, 5, 6, 8-10, 14, 15, 17, 18 and 21 are currently pending in the application. No new matter has been added by these amendments.

On pages 2-7 of the Office Action, the Examiner rejected claims 1, 5, 6 and 8-21 under 35 U.S.C. § 103(a) as being unpatentable over Takizawa (US 6,504,254). For the reasons discussed below, it is respectfully submitted that the present claims, including independent claims 1, 9 and 14, are clearly patentable over the prior art of record.

Amended independent claim 1 recites a semiconductor device which includes a semiconductor substrate having a pattern forming region and a pattern non-forming region, a wiring pattern formed on the pattern forming region, and a plurality of dummy patterns formed on the pattern non-forming region, with the plurality of dummy patterns being formed within a plurality of dummy areas, and with each of the plurality of dummy areas having a same shape. Claim 1 also recites that *each of the dummy patterns has a plurality of parallel line patterns, each of the line patterns of the plurality of line patterns being spaced apart from each other* by an area filled by the deposition of said insulating film. Claim 1 also recites that a distance between each of the line patterns of the plurality of line patterns is less than 72 μm.

Takizawa discloses hexagonal-shaped dummy wiring sections 30 having an opening 32 (Fig. 2) or a plurality of openings 32 (Fig. 4). However, Takizawa does not disclose that *each of the dummy patterns has a plurality of parallel line patterns, with each of the line patterns of the plurality of line patterns being spaced apart from each other*, as required by amended independent claim 1. In this regard, it is noted that on page 2 of the Office Action, the Examiner indicates that line segments 32 in Fig. 4(b) of Takizawa correspond to the plurality of line patterns of the present invention. However, it is noted that line segments 32 intersect each other, and are therefore not parallel line patterns as required by independent claim 1. Therefore, Takizawa does not disclose that each of the dummy patterns has a plurality of parallel line

patterns because Takizawa only discloses intersecting line patterns.

Amended independent claim 9 recites a semiconductor device which includes a semiconductor substrate having a pattern area and a non-pattern area, a conductive pattern formed on the pattern area of the semiconductor substrate, and a plurality of dummy patterns formed on the non-pattern area of the semiconductor substrate, with each of the plurality of dummy patterns having a same continuous rectangular outline shape as each other and being arranged in a matrix with predetermined spacing. Claim 9 also recites that *each of the dummy patterns has a single square-shaped opening* so that a pattern ratio of the semiconductor device is reduced. Claim 9 also recites that a width of the opening of each of the dummy patterns is less than 72 μm.

As discussed above, Takizawa discloses hexagonal-shaped dummy wiring sections 30 having an opening 32 (Fig. 2) or a plurality of openings 32 (Fig. 4). However, Takizawa does not disclose that *each of the dummy patterns has a single square-shaped opening*, as required by amended independent claim 9. It is noted that Fig. 4(c) of Takizawa discloses a dummy wiring section which includes square-shaped openings. However, Takizawa discloses a dummy wiring section which includes four square-shaped openings, and therefore does not disclose dummy patterns which each have a single square-shaped opening.

Amended independent claim 14 recites a semiconductor device which includes a semiconductor substrate having a pattern area and a non-pattern area, a conductor pattern formed on the pattern area of the semiconductor substrate, and a plurality of dummy patterns formed on the non-pattern area of the semiconductor substrate. Claim 14 also recites that each of the dummy patterns has a space portion within each of the dummy areas so that a pattern ratio of the semiconductor device is reduced. Further, claim 14 recites that each of the dummy patterns includes an opening at the space portion, with the opening having a shape of a character, with each opening of the dummy patterns having a width less than 72 μm.

As discussed above, Takizawa discloses hexagonal-shaped dummy wiring sections 30 having an opening 32 (Fig. 2) or a plurality of openings 32 (Fig. 4). However, Takizawa does not disclose that *each of the dummy patterns includes an opening at the space portion, with the*

opening having a shape of a character, as required by amended independent claim 14. In this regard, it is noted that Takizawa discloses triangular openings (Fig. 4(b)) and square-shaped openings (Fig. 4(c)), but does not disclose openings having the shape of a character, as required by claim 14.

Therefore, it is respectfully submitted that amended independent claims 1, 9 and 14, as well as claims 5, 6, 8, 10, 15, 17, 18 and 21 which depend therefrom, are clearly allowable over the prior art of record.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice to that effect is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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